Application Note AP-55

Guidelines for RC5035/36 Motherboard Designs

Introduction

The next generation of microprocessors will pack in more functions and more flexibility to perform the complex tasks required by today's demanding applications. The Pentium® microprocessor architecture is supplanting the X86 architecture as the trend towards more multimedia applications and the Internet rapidly evolves. This evolution has demanded increasing numbers of transistors be integrated onto a single chip, with the current Pentium chips integrating well over 5 million transistors on a single piece of silicon. In order to achieve this kind of density, the physical geometry of each transistor has been reduced to the sub-micron level and with each successive design geometry shrink, the corresponding voltage that the transistor can operate over has been reduced as well. This trend in processor design is proceeding at a rate that has outstripped the system's ability to cope with the changing supply voltage requirements. The majority of the logic, control, and memory chips are now operating off of a 3.3V supply. This voltage is reduced from the 5V supply of 5 years ago.

With the new higher speed Pentium CPUs, the voltage of the “core” logic is trending lower than the 3.3V that is powering the other parts of the system while the average current requirement is increasing. (see Table 1) This trend is creating the demand for fast, flexible, and efficient power supply systems capable of supplying both the 3.3V power for the I/O portion of the CPU as well as the lower voltage “core” portion of the CPU. No longer can the computer designer simply provide the lower voltage from a linear regulator. This application note will describe a flexible and efficient dual power supply system and its implementation for supporting the P55 Pentium CPU.

P55C Overview

The P55C is the third generation of Pentium class microprocessors. It has many feature enhancements that allow the P55 to integrate higher performance and is yet pin compatible with the older Pentium processors. The single most significant feature of the P55C relative to the older generation processors is the requirement for a dual power supply. The P55C power supply is divided into two sections, one supply powers all of the I/O circuitry that is required to interface with the external support chips on the motherboard, usually 3.3V. The other power supply is required to provide a lower voltage to the CPU core circuitry, typically 2.5 – 2.9V. The motherboard for this application will have to have a dual power plane system as shown in Figure 1 on the next page.

Table 1 CPU Voltage/Current Requirements

Processor	Description	Voltage Required	Current Required
P54	Core & I/O Chipset 512k SRAM	STD 3.3V (3.135–3.60V) VRE 3.5V (3.4–3.6V)	5A 1A 1A 7A
Cyrix 6x86	Core & I/O Chipset 512k SRAM		7.2A 1A 1A 9.2A
P55	Core	2.8V±100mv	5.7A
	I/O Chipset 512k SRAM	STD 3.3V (3.135–3.60V)	.4A 1A 1A 2.4A

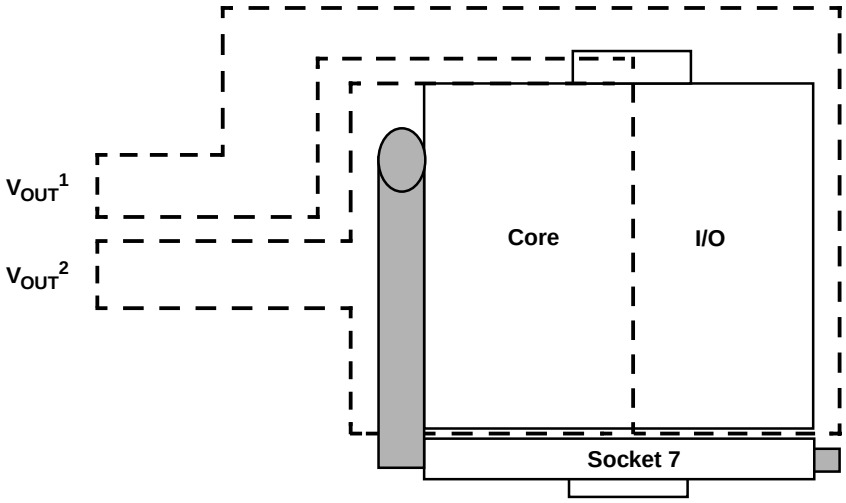

Figure 1. Dual Power Plane with Socket 7 for P55C

The P55C has a pin defined on the Socket 7 called VCC2DET. This pin will be used to steer the voltage of the core power plane to the correct voltage depending upon the CPU installed on the socket. The P55C will assert this pin LOW and cause the on board regulator to provide the lower voltage for the core power plane.

P54/P55 Flexible Motherboard

The flexible motherboard concept allows for a variety of processors to be supported by a single motherboard design. An auto-configurable regulator circuit is one option for such a motherboard design. This approach would have to allow for the 3.3V Standard Range, the VRE* s-specification, P55C, and the OverDrive processors to be easily supported without the need for any external jumper configurations.

Figure 2 shows how the RC5035/36 would implement an auto-configurable voltage regulator system configuration.

The P55C has a pin defined on the Socket 7 as VCC2DET. This pin is used to steer the correct voltage to the CPU core voltage plane depending upon which processor is installed in the socket. On the P54 Pentium processors and OverDrive processors, this pin is an internal no connect and therefore can be pulled up to a high level by an external pullup resistor. On the P55C, this pin is always connected to a low. For the 3.3V or VRE s-spec. Pentium processors, both the switching and the linear regulator portion of the RC5035/36 can be driven to either 3.3V or 3.5V in the current sharing configuration or alternatively, the linear regulator can be disabled, while the switch-mode regulator supplies the entire current load for the processor.

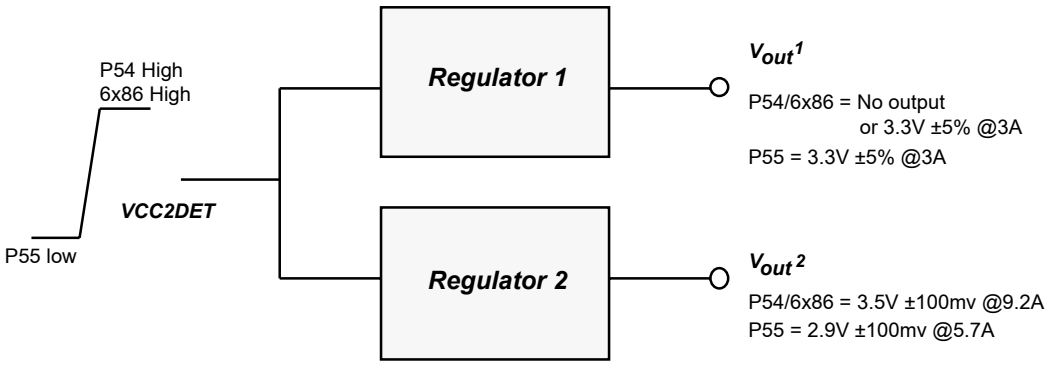

Figure 2 P54/P55 Auto-Configurable Regulator

*Implementation Guidelines for 3.3V Pentium Processors with VR/VRE Specifications, Dec. 1994

RC5036 Dual Regulator for P55C

Overview

The RC5036 combines a highly efficient switch-mode DC-DC converter with a precision linear regulator in a single 16 SOIC package. With the appropriate external components, the RC5036 can be configured to meet the requirements for the P54/P55C Flexible Motherboard. Within this design is the integration of the complete control logic for utilizing the VCC2DET pin of the P55C processor (see Figure 3 below). Utilizing this control function, allows the RC5036 to be auto-configured between the 2.8V core voltage for the P55C and the 3.5V VRE s-spec. voltage for the P54.implement a dual power supply system with the capability to supply both the “core” voltage as well as the I/O voltage for a dual voltage CPU such as the Pentium P55C.

Functional Description

Main Control Loop

The RC5035/36 contains a precision trimmed zero TC reference, a “constant-on-time” architecture controller, a high current output driver, and a low offset op-amp. The block diagram shown if Figure 3 shows how the chip combines with the external components to form an adjustable dual power supply. The main control loop for the switch-mode converter consists of a pair of signal conditioning amplifiers that take the raw voltage and current information from the regulator output, compare them against the precision reference and present the error signal to the input of the “constant-on-time” oscillator. The current feedback controlling signals come from across the Iout sense resistor to the Ifbh and Ifbl inputs to the RC5035/36. The voltage feedback signal is sent back from the output through a voltage divider to the FBSW pin of the chip to compare against the precision reference. The error signals from both the current feedback loop and the voltage feedback loop are summed together and used to control the off -time portion of the “constant-on-time” oscillator. The current feedback error signal is also used to provide short circuit protection for the RC5035/36.

Linear OP-Amp

The low-offset op-amp is configured to be the controlling element in a precision low-drop-out linear regulator. As can be seen from Figure 3, the op-amp is used to compare the divided down output of the linear regulator to the precision reference. The error signal can be used then to control either an N-channel Low Rdson FET or a power NPN transistor.

High Current Output Drivers

The RC5035/36 high current output driver contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of pumping out 1A of current in less than 100ns. The driver's power and

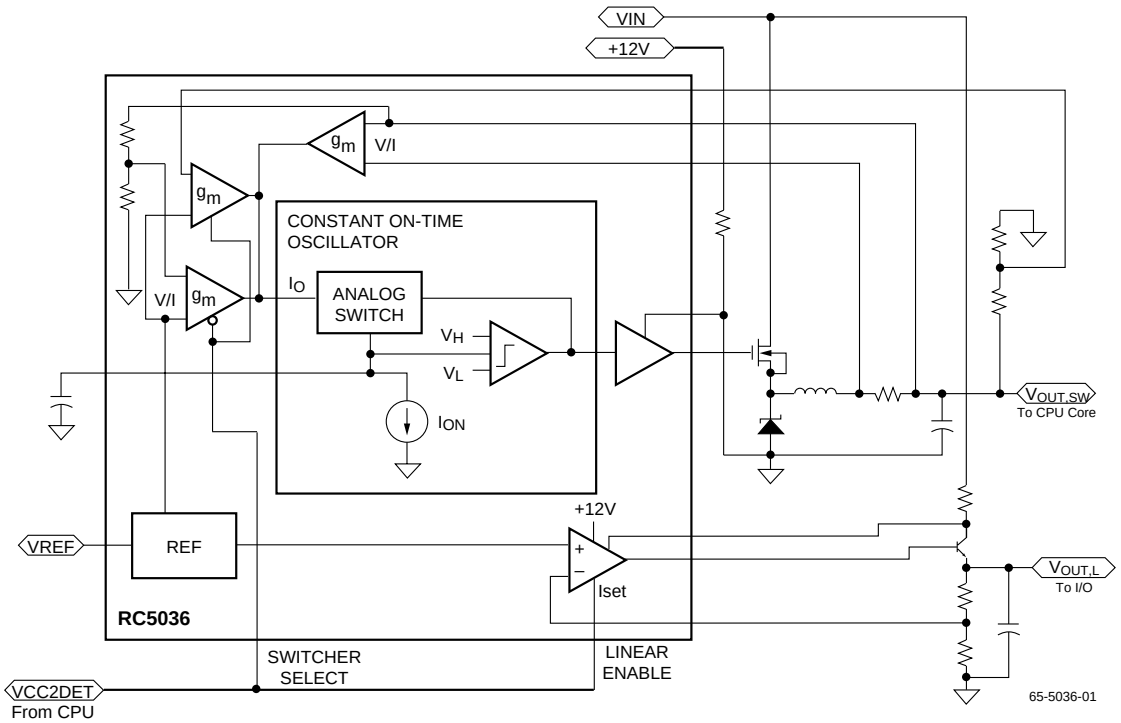

Figure 3 RC5036 Block Diagram

ground are separated from the overall chip power and ground for added switching noise immunity. The VOSW driver has a power supply, VCCP, which can be derived from an external 12V source or boot-strapped with a capacitor. In the boot-strapped mode, C2 is connected to the source of M1 and is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCP voltage equal to 2*VCC – Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the gate drive to the external MOSFET that will be needed for achieving a low Rdson. If VCCP is derived from an external 12V source, the Rdson is assured of being low due to the increased gate drive voltage to the power FET M1.

Internal Reference

The reference in the RC5035/36 is a precision band-gap type reference set to 1.5V. Its temperature coefficient is trimmed to provide a near zero TC. For applications that require a different voltage, a pair external resistors can be used change the output voltage from 1.5V up to 3.6V. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over-Voltage Protection

The RC5035/36 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5035/36 will shut down the output drive signals to the power FETs.

Oscillator

The RC5035/36 oscillator is designed as a fixed on-time, variable off-time oscillator. It is comprised of a window comparator, a fixed current source, an analog switch and an external timing capacitor. The oscillator will exhibit a fixed on-time, where the off-time will vary proportional to the feedback current from the switched-mode regulator. Therefore, the overall switching frequency of the oscillator will vary with the load current. The window comparator is used to provide the constant on-time, where the analog switch opens when the upper comparator threshold limit is reached. A fixed current source then discharges the oscillator capacitor until the lower comparator threshold is reached. Therefore, the fixed on-time is derived from a constant current slewing a fixed capacitor through a constant voltage. The comparator output directly feeds the output driver circuitry, eliminating the need for logic circuitry in the PWM. Once the comparator input reaches the low threshold, the comparator output switches levels and enables the analog switch. The feedback current then forces the output to slew up to the comparator upper threshold. Using this implementation, lighter loads and/or smaller error voltages will increase the time to reach the upper comparator threshold and thus increase the overall switching frequency.

RC5035 Dual Regulator

The RC5036 is a special case of dual regulator that was derived from the general dual regulator, the RC5035. As shown below in Figure 4, the RC5035 is identical with the RC5035 with the exception of the built in switching function that allows for use with the P54/P55 Flexible Motherboard design.

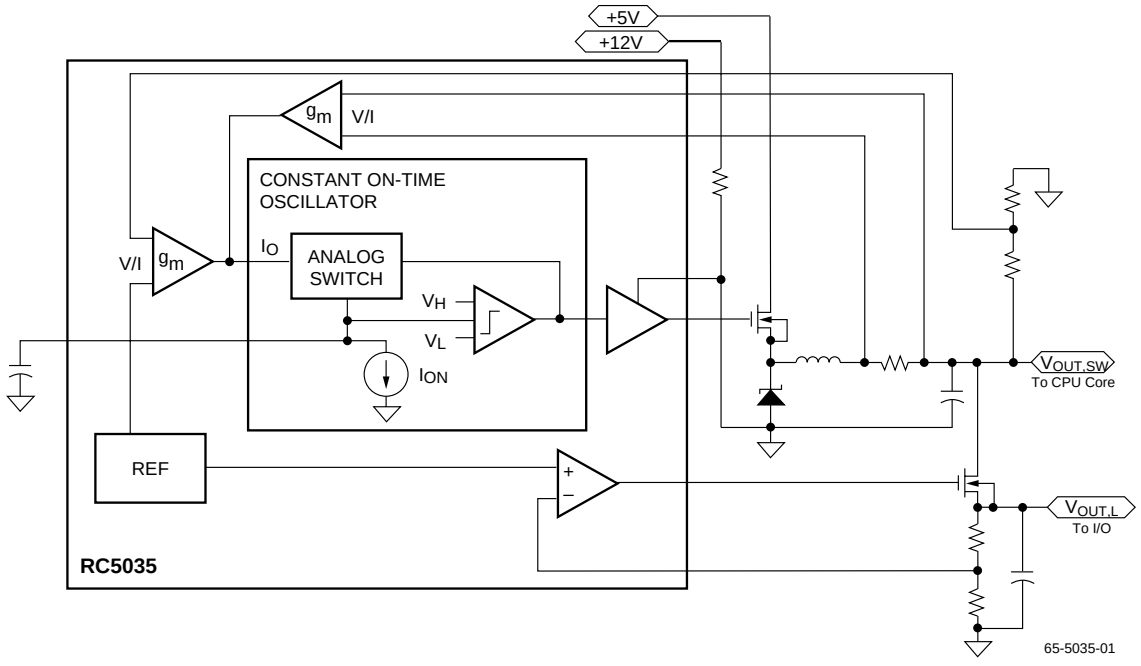

Figure 4 RC5035 Block Diagram

RC5035/36 Evaluation Board

Fairchild provides an evaluation board for the purpose of verifying the data sheet specifications as they relate to the system level performance of the RC5035/36. The evaluation board is not intended to be a complete motherboard solution, but rather serve as a guide as to what can be expected in performance with the supplied external components and PCB layout. Appendix B contains the schematic, BOM, and the complete layout of the evaluation board as a reference.

Dual Power Supply Application

Although most of today's desktop computers use multiple output power supplies, the lower operating voltages and increased requirements for low transient response have necessitated the move into local power supply systems with their inherent advantages of lower parasitic inductance and resistance. The RC5035/36 is designed to specifically address the need for a localized dual power supply for the P55C.

P55C

The P55C Pentium processor has twice the L1 cache memory of the previous P54 Pentium processor and includes some other refinements in architecture to achieve higher performance levels with multimedia applications.

The operating frequency of the core is rated at 150 and 166MHz, with the core supply voltage going down to the 2.5–2.9V range. The P55C, in order to remain compatible with the other previous processors, will have an I/O voltage of 3.3V to provide complete compatibility with existing system chipsets and SRAMs. The core current requirement is specified to be 3A at 2.5V, while the I/O is specified to require 0.4A at 3.3V. However, there will be other chips that will require current from the 3.3V supply such as the I/O chipset (typically less than 1A) and the DRAMs.

The preferred embodiment of the RC5035/36 dual regulator is to use the switch-mode regulator to provide the 2.X voltage supply for the core, while the linear regulator can provide the less critical 3.3V power supply for the I/O portion of the design. Figure 5 shows a typical dual power supply configuration. Using the switch-mode regulator for the core voltage supply has two advantages. First, since the core voltage is dropped to below 3V, the high efficiency switch-mode regulator will reduce the power dissipation requirements of the power FETs at high currents, and second, the built in over-voltage protection inherent in the switch-mode design will serve to protect the CPU core from any voltage related stresses. The linear regulator can easily handle the 5V to 3.3V conversion at the lower currents without creating a large burden on the system designer for thermal management.

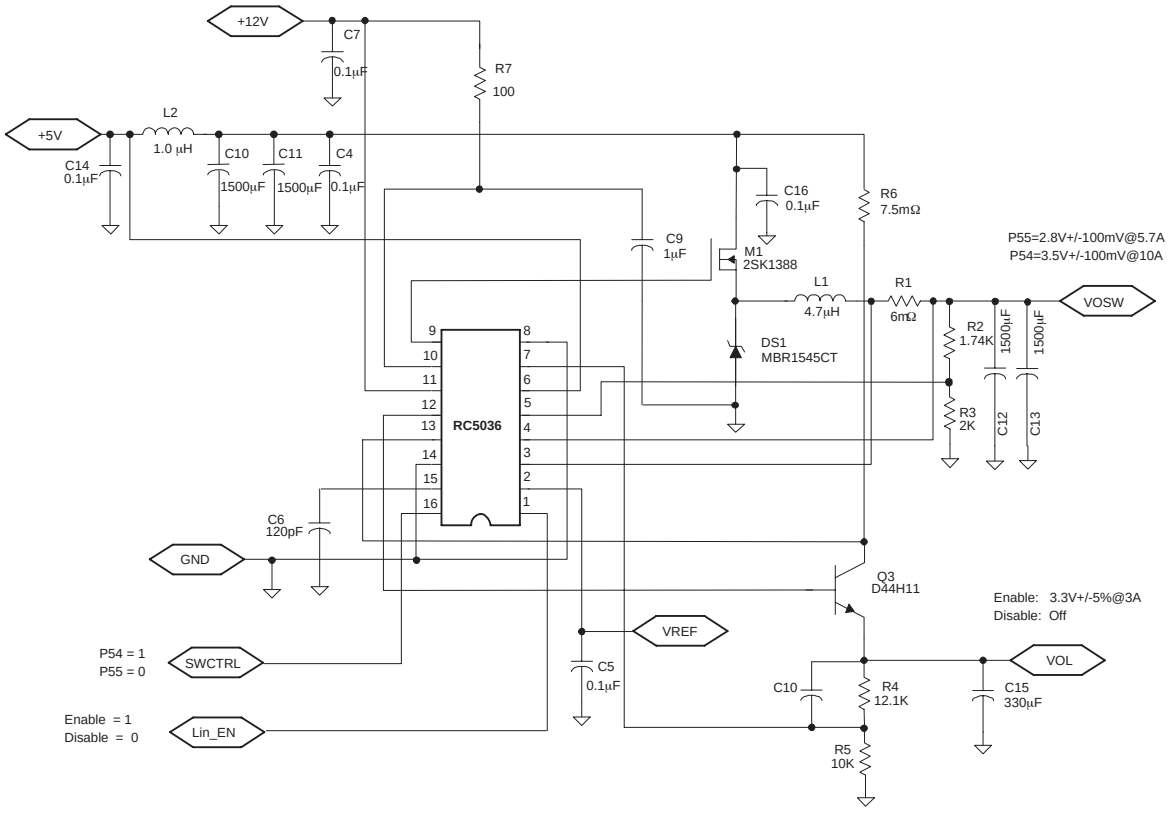

Figure 5 Dual Power Supply for P54/P55C Flexible Motherboard

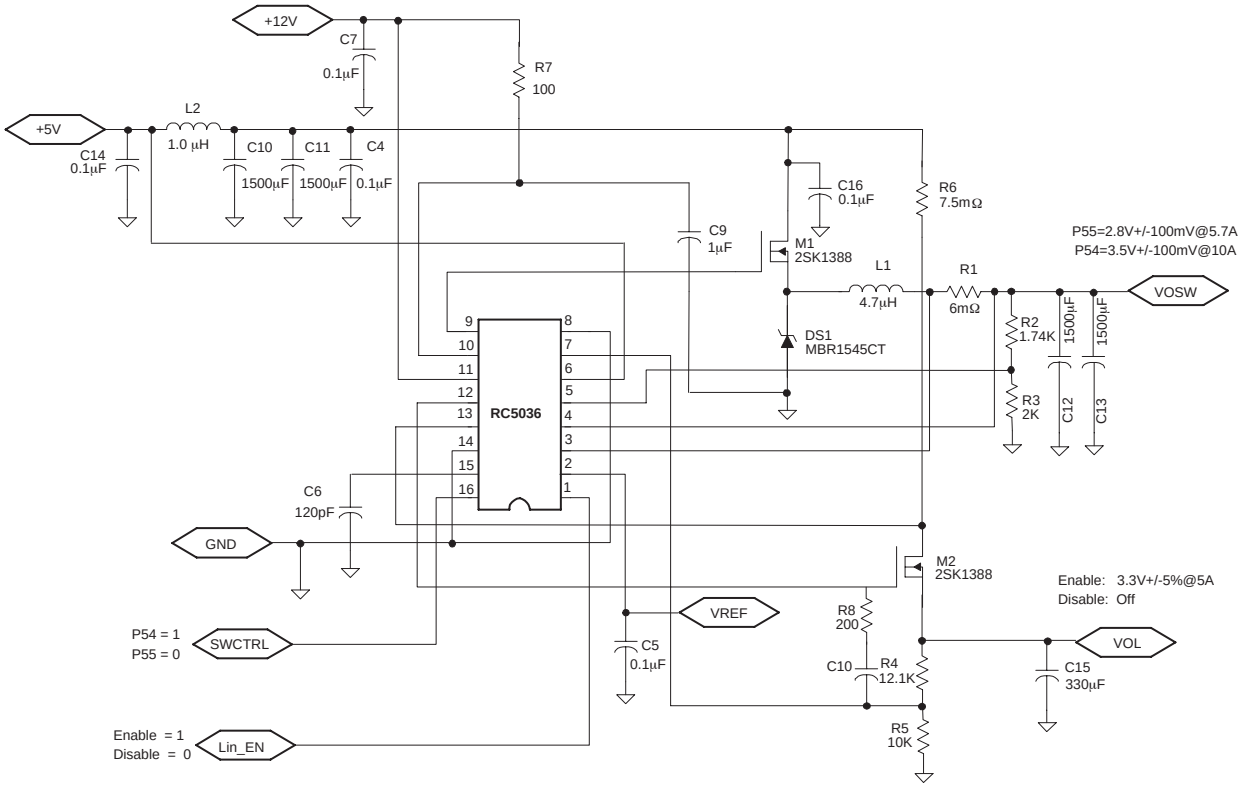

Figure 6 RC5036 Application for P54/P55C with FET

A third application of the RC5035/36 linear regulator is to use it as a low-drop-out regulator slaved off of the RC5035/36 switching regulator. An example of this application would be shown in the schematic of Figure 7. The RC5035/36 switching regulator is used to provide a high efficiency conversion from 5V to 3.3V, while the linear regulator is used to drop the 3.3V down to 2.8V or lower. This approach has the advantage of reducing the power dissipation of the linear regulator FET substantially, to the point that it would not require a heat sink. The disadvantage of this approach is that the switching regulator must carry the load current for both the switching output as well as the linear output. In the case of P55, the linear regulator would be supplying the higher current required by the processor core, rather than the switching regulator in the application of Figure 5. The second disadvantage of this approach is that the switching regulator would be required to provide the short circuit current protection for both the switcher and the linear regulator, the linear short circuit protection would need to be disabled. The linear regulator short circuit protection is achieved by using a differential amplifier with two inputs; one input is connected to the chip +5V supply, the second input is from the VSC2 pin. Since the majority of applications would have the linear regulator dropping from the +5V supply, the short circuit amplifier is referenced to the 5V supply rail. Thus, if the input to the power transistor for the linear regulator comes from any supply other than the +5V, the linear short circuit protection function cannot be used.

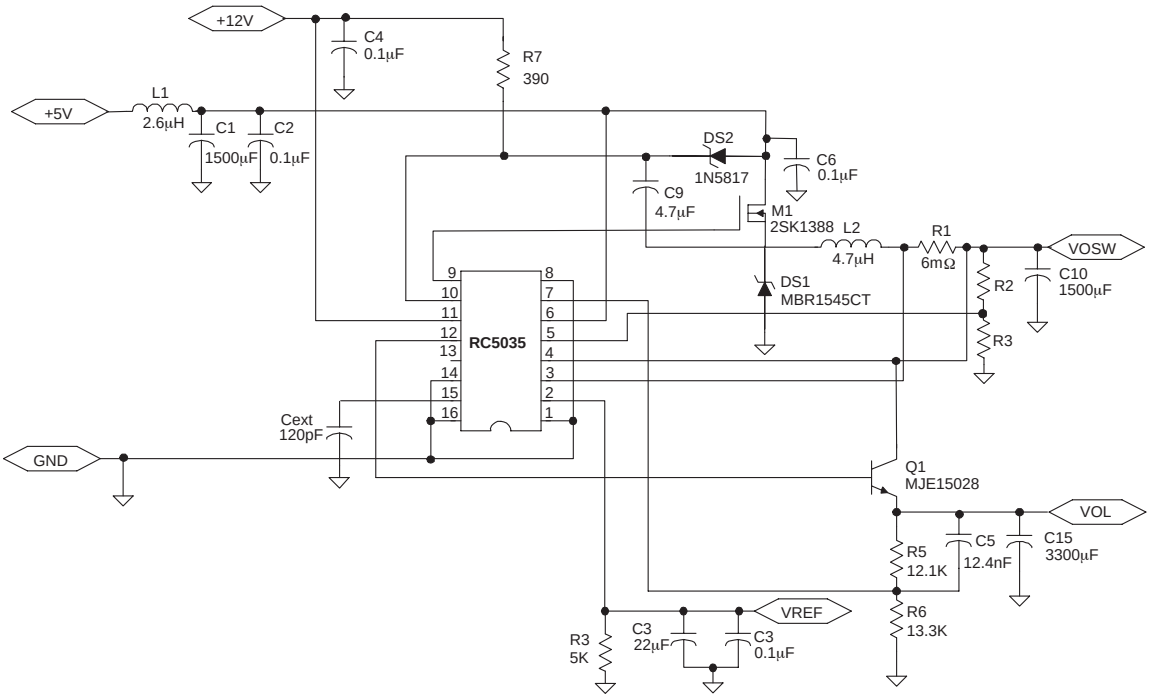

Figure 7 RC5035/36 with Linear Regulator Slave

The circuit shown in Figure 8 details the later implementation where the regulator is either a single switch-mode operating at 3.3 or 3.5V, or upon detection that the VCC2DET is low, the RC5035/36 implements a dual supply regulator addressing the P55C. In this configuration, the design should allow for the switch-mode regulator to carry the highest current for the various processors under consideration, and the linear should be designed to supply only what is required to support the P55C processor I/O plus peripheral chips that may run off of 3.3V.

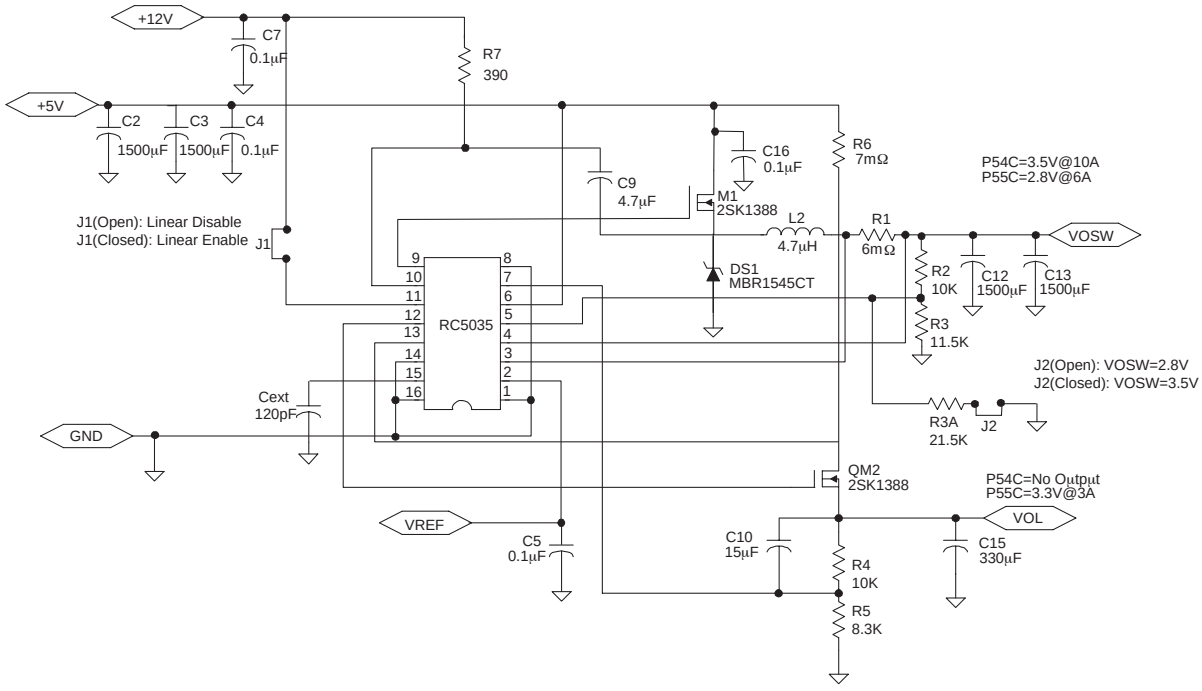

Figure 8 RC5035 Implementation for P54/P55C Flexible Motherboard

Detailed Design Relationships

Generalized Design Equations

The derivation of the basic step-down buck regulator design equations will serve as the basis for the design relationships for the RC5035/36. Figure 9 shows the basic step-down DC-DC converter without a feedback controller.

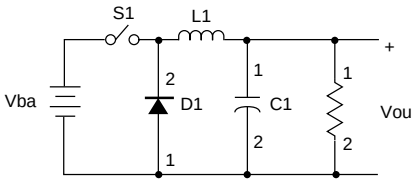

Figure 9 Simplified Step-Down DC-DC Converter

The basic operation follows in two steps. Step one occurs when switch S1 is closed. When this occurs, the input voltage is impressed upon the inductor L1. The current flowing in the inductor can be calculated from the following relationship (assuming an ideal switch):

$$V_{IN} - V_{OUT} = L1\frac{(I_2 - I_1)}{T_{ON}}$$

When switch S1 is open, the diode D1 will conduct the current through the inductor, and the current through the inductor will decrease at the rate shown below:

$$V_D + V_{OUT} = L1\frac{(I_2 - I_1)}{T_{OFF}}$$

By rearranging these two equations, we can arrive at the basic relationship for the step-down buck regulator shown below. These equations are valid for the assumption that the regulator is operating in the continuous mode. There are other design equations for a regulator operating in the discontinuous mode but we will not address those here. Figure 10 shows a pictorial representation of the voltage and current relationships described for the step-down regulator.

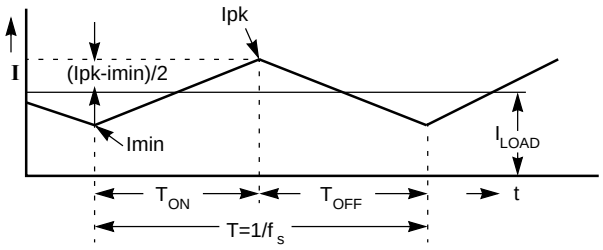

Figure 10 Inductor Current Relative to Period

$$\frac{V_{OUT} + V_D}{V_{IN} + V_D} = \frac{TON}{T} = DutyCycle$$

Where T is the total period of the clock, $T_{ON} + T_{OFF}$.

Specific Design Equations

The above general relationships serve as the basis for the specific design relationships used in selecting the proper inductance and capacitance for the design under consideration.

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), maximum DC current (I_O), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade-offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship:

$$P_{LOSS} = I^2 \times R_{DC}$$

Where I is the average load current in the inductor and R_{DC} is the DC resistance of the inductor.The value of the inductor is a function of the switching frequency (T_{ON}) and the maximum inductor current, I_{PK}. The max inductor current can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_O}{L}\right)T_{ON}$$

Where T_{ON} is the maximum on time of the M1 FET and V_{SW} is the drain-to-source voltage dropped by the FET. Then the inductor value can be calculated with the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right)T_{ON}$$

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5035/36 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5035/36 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

Where: $I_{MAX} = I_{PK} * 1.2$

Since the value of the sense resistor is generally in the milliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the RC5035/36 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

Feedback Voltage Divider

The RC5035/36 precision reference is trimmed to be at 1.5V nominally. This is done so that the RC5035/36 allows the system designer complete flexibility in choosing the output voltage for each regulator from 1.5V up to 3.6V. Therefore, the design procedure includes the setting of the feedback resistors. These resistors should be 0.1% accurate resistors to obtain the best accuracy results. The value of the resistors is also an important consideration; choosing the total resistance of the divider network incorrectly can negate the effect of using 0.1% resistors. The following equations relate the output voltage to the reference voltage.

Linear Regulator

$$V_{OUT} = V_{REF}\left(\frac{R2 + R3}{R3}\right)$$

Switching Regulator

$$V_{OUT} = V_{REF}\left(\frac{R4 + R5}{R4}\right)$$

Since the voltage reference for the RC5035/36 is 1.5V, then the equation becomes:

$$V_{OUT} = 1.5V\left(\frac{R4 + R5}{R4}\right)$$

Assuming that R4 is the resistor connected between the feedback pin of the RC5035/36 and ground, then we will pick V_{OUT} to be 3.3V and re-arrange the equation to solve for the resistor values.

$$R5 = R4\left(\frac{3.3 - 1.5}{1.5}\right) = 1.2(R4)$$

Thus if we were to select 50K as R4, then R5 would be 60K. However, we are not finished at this point. Since the voltage divider goes to the input of a bipolar op-amp inside the RC5035/36, we must consider the effect of the input current on the accuracy of our voltage divider network. If the input bias current of the op-amp were to be on the order of 1µA, we can calculate the effect of the current by finding the total bias current required for the divider network.

$$I_{NET} = \frac{3.3V}{50K + 60K} = 30\mu A$$

A 1µA input current would yield a 3.3% error in the output voltage due to the input current required for the RC5035/36 op-amp. Thus, the 50K and 60K resistors would not be a good choice. Were we to reduce the resistors by a factor of 10, to 5K and 6K, then the 1µA input current would produce only a 0.3% error and would be acceptable.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5035/36. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. Low “ESR” capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation:

$$ESR = \frac{DF}{2\pi fc}$$

Where DF is the capacitor's dissipation factor, f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. An estimate of the bulk decoupling capacitance required can be done by using the following equation:

$$C = \frac{I \times \Delta t}{\Delta V - I \times ESR}$$

Where: Δt is the period over which the CPU will demand current from the capacitors

ΔV is the maximum allowable voltage change over that period

Schottky Diode Selection

The application circuit of Figure ?? shows a schottky diode, DS1. It is important in the selection of DS1 that it have a low forward voltage drop as this directly affects the regulator efficiency. During the off time of the power FET, M1, the voltage on the inductor will drop until the diode DS1 clamps and conducts the full current in the inductor. The power in DS1, $P_D = V_F \times I_L$, is a direct subtraction from the overall efficiency of the DC-DC converter; therefore, it is important for DS1 to have a low V_F in order to minimize the power loss term. A diode selection guide is given in Appendix C for some commonly available schottky power rectifiers.

MOSFET Switches

The MOSFET switch in the RC5035/36 applications circuit is an N-channel “logic-level” FET. This means that it will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest Rdson at the given Imax current level. The value of Rdson directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5035/36. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. A selection guide for logic-level MOSFETs is given in Appendix C to help in selecting the appropriate FET for each application.

Timing Capacitor

Selecting the appropriate timing capacitor for the application is accomplished by looking at the design trade-offs between frequency, maximum expected load current, efficiency and response time. In general, the frequency, response time and efficiency are all inter-related. However, since the RC5035/36 relies on a constant-on-time control for the PWM function, the maximum load current also comes into play. To review the operation of the constant-on-time PWM, we know that the function of the PWM controller is to modulate the current switch in such a manner so as to provide the correct current ramp in the inductor.
The amount of charge and discharge in the inductor determines what the average load current will be at any given time. The RC5035/36 modulates the current switch by adjusting the off-time in response to the feedback inputs obtained from the regulator output. This means that in response to varying load conditions, the RC5035/36 will adjust the frequency of the oscillator in order to modulate the off-time of the FET. Thus for a given increasing current load, the RC5035/36 will try to increase the frequency in order to dump more charge into the inductor (see Figure 11).

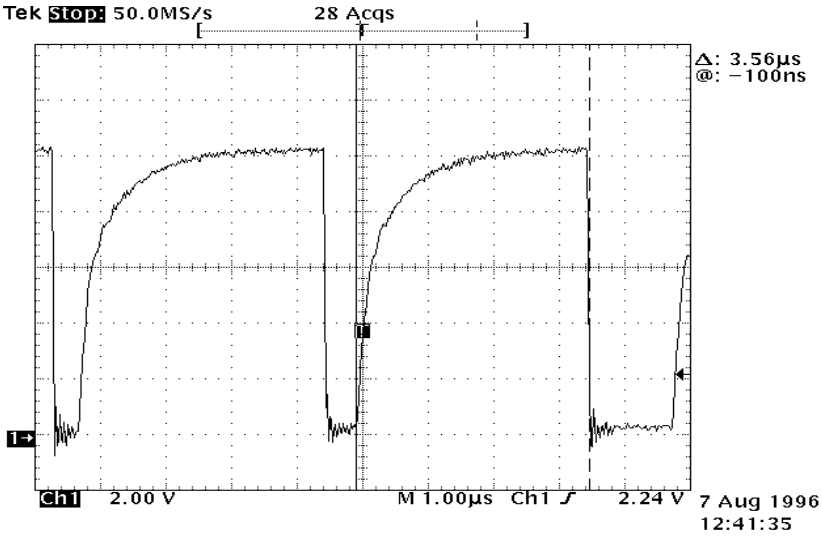

Figure 11 Scope Photo of pin 9 at a 5Amp load

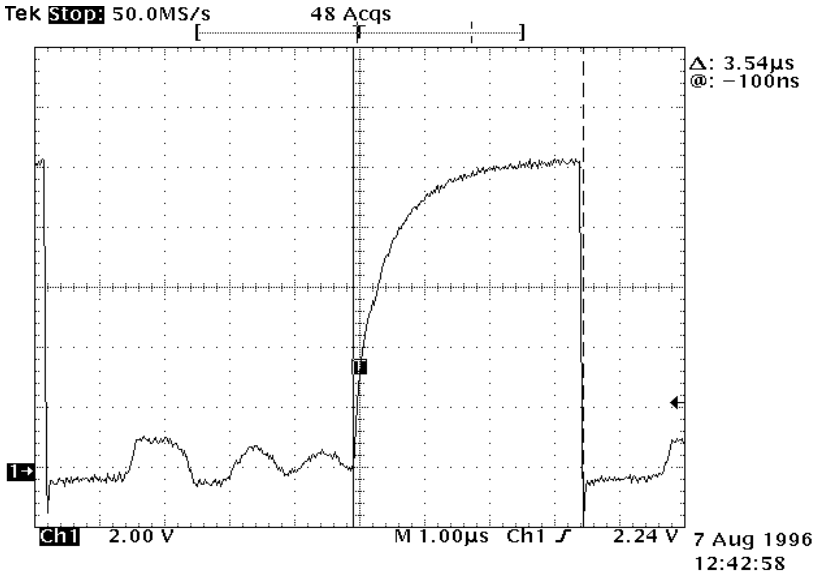

Figure 12 Scope Photo of pin 9 at a 0.1A load

Conversely, as the current load is reduced, the RC5035/36 will adjust the oscillator frequency down in order to maximize the FET off-time. (see Figure 12) This will ultimately place an upper and lower bound on the operating frequency of the RC5035/36 oscillator.

Figure 13 shows the relationship between the nominal oscillator frequency and the C_{EXT} capacitance. In general, the lower the oscillator frequency(larger C_{EXT}), the better will be the overall efficiency of the design. However, load regulation and response time will suffer. The higher the oscillator frequency, the better will be the transient response time and the load regulation. Thus these factors must all be weighed together when deciding the appropriate C_{EXT} capacitor.

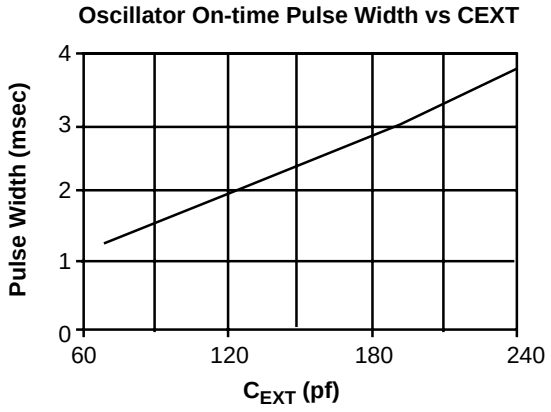

Figure 13 Pulse Width vs Capacitance

Linear Regulator Design Considerations

The RC5035/36 linear regulator can be configured in several ways depending upon the application requirements. For delivering light loads (up to 3A), the most cost effective solution is to use an NPN bipolar transistor as the high power pass element. This can be used effectively to provide 3.3V from a +5V supply as shown in Figure 2 above. The considerations when using this approach involve the output current capability of the linear regulator op-amp as well as the thermal dissipation of the RC5035/36/36 in the 16 SOIC package. The bipolar transistor should have a Beta that is > 80 in order to limit the base current required from the RC5035/36 linear op-amp. If we perform a thermal analysis on the application described in Figure 2 above we will arrive at the underlying reasons for the design requirement of a greater than 80 Beta.

For reliability, we require that the junction temperature not exceed 120°C, thus we can calculate the maximum power dissipation allowable for the 16 SOIC package:

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\Theta JA}}$$

Where if we assume that the ambient temperature T_A is 50°C and the thermal resistance of the 16 SOIC package is 150°C/W, then the maximum power dissipation for the RC5035/36 is:

$$P_D = \frac{120 - 50}{150} = 0.466W$$

Using a typical power transistor, for example the D44H11 (available from several manufacturers), we find that the minimum Beta for operation a 3A will be around 50 at 25°C. At first glance, we might think that this violates our above requirement of Beta >80, however, further analysis will show that the Beta in the actual application will be much higher. We know that over temperature the Beta will increase. Thus if we calculate junction temperature of the power transistor under a 3A load, we will get:

$$P_D = I \times V_{CE} = 3A \times (5 - 3.3) = 5.1W$$

Using the equation from above for obtaining the junction temperature, we have:

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\Theta JA}} = 5.1W$$

For a TO-220 package with the appropriate heat sink, the $R_{\Theta JA}$ is about 8°C/W. If we again assume that the ambient temperature is 50°C, the we can solve for $T_{J(max)}$.

$$P_D \times R_{\Theta JA} + T_A = T_{J(max)} = 5.1W \times 8 + 50 = 90.8°C$$

Thus the transistor Beta will be much higher than the minimum and a transistor with a rated Beta minimum of 50 at 25°C should yield us a Beta of 80+ under the above ambient conditions. Now we can calculate the RC5035/36 power dissipation due to the base current required by the NPN bipolar transistor, assuming a minimum Beta of 80. At the maximum load of 3A, the base current will be 3/80=37.5mA. Since the output of the transistor is at 3.3V, the base voltage will be one diode drop higher, 3.3 +0.7=4V. Thus, if the RC5035/36/36 VCCL supply (the VCC supply for the op-amp) is connected to 12V, then the power dissipation of the RC5035/36/36 due to the linear regulator is:

$$P_D = (12V - 4V) \times 37.5mA = 0.3W$$

Thus we can see that at the maximum current of 3A, the power dissipation of the RC5035/36/36 will be within the maximum power allowed at an ambient temperature of 50°C.

An alternative approach to using the power NPN transistor would be to simply replace it with an N-channel power MOSFET. This application completely eliminates the thermal concerns for the RC5035/36 package since the FET requires no current other than during a transient period. Then the burden of the thermal requirement is placed on the FET. This is the recommended approach for currents that exceed 3A.

Motherboard Design Considerations

Modern high speed computers require careful attention be paid to all aspects of PC Board design, both electrical and thermal. With I/O bus speeds at 66MHz and power supply currents in the 10 Amp range, each phase of the motherboard design requires careful attention be paid to the parasitic resistance and capacitance on the PCB.

Electrical Design Considerations

A dual power plane design presents a variety of challenges in design, especially if the same plane is to be split to serve both the core voltage and the I/O. Care must be taken to insure that the planes have adequate area for the currents that will be flowing to the CPU. The RC5035/36 needs to be located fairly close to the CPU in order to reduce the IR drop. And when designing with any switch-mode regulator, minimization of trace lengths to reduce RF noise is a must. This is especially true for the high frequencies of the RC5035/36. Most of the design problems that are associated with switch-mode regulator have their roots in the initial component placement. The following guide should serve as a step-by-step procedure to follow when designing with the RC5035/36.

RC5035/36 Placement

The RC5035/36 should be placed as close to the Vcore side of the P55C as possible. It is preferable to have the PC layer that is directly underneath the RC5035/36 be the ground layer. This serves as extra isolation from the noisy power planes.

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed in such a way as to minimize the length of the gate drive signal from the RC5035/36. Excessive lead length on this trace will cause high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise will be very difficult to suppress. This trace should be routed on one layer only and kept well away from the “quiet” analog pins of the device; VREF, CEXT, FBSW, IFBH, IFBL, and VFBL. (see Figure 14)

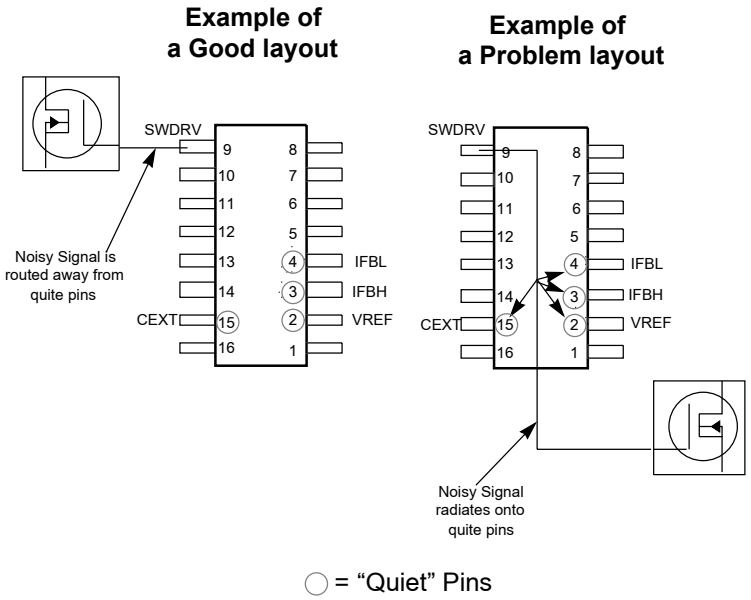

Figure 14 Example of “Good” vs “Bad” Placement

Inductor and Schottky Diode Placement

The inductor and fly-back schottky diode need to be placed close to the source of the power MOSFET for the same reasons as above. This node will swing between the drain voltage of the FET and the forward voltage of the schottky diode. It is recommended that this node be converted to a plane if possible. This node will be part of the high current path in the design, and as such it is best treated as a plane in order to minimize the parasitic resistance and inductance on that node. Since most PC board manufacturers utilize 1/2 oz. copper on the top and bottom signal layers of the PCB, it is not recommended to use these layers to rout the high current portions of the regulator design. Since it is more common to use 1oz copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

Capacitor Placement

One of the keys to a successful switch-mode power supply design is correct placement of the low ESR capacitors. Decoupling capacitors must serve two purposes; first there must be enough bulk capacitance to support the expected transient current of the CPU, and second, there must be a variety of values and capacitor types to provide noise suppression over a wide range of frequencies. The low ESR capacitors on the input side (5V) of the FET must be located close to the drain of the power FET. Again here, minimizing parasitic inductance and resistance is critical in suppressing the ringing and noise spikes on the power supply. The output low ESR capacitors need to be placed close to the output sense resistor to provide good decoupling at the voltage sense point.

One of the characteristics of good low ESR capacitors is that their impedance gradually increases as the frequency increases. Thus for high frequency noise suppression, good quality low inductance ceramic capacitors need to be placed in parallel with the low ESR bulk capacitors. These can usually be 0.1uF 1206 surface mount capacitors.

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1uF directly on the pin of the RC5035/36. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCL pin that connects to +12V, though this one is somewhat less critical since it powers only the linear op-amp. Each ground should have a separate via connection to the ground plane below.

Thermal Design Considerations

Good thermal management is also critical is the design of high current regulators. System reliability will be degraded if the component temperatures become excessive. The following guide should serve as a reference in designing for good thermal management.

MOSFET Temperature

The power dissipation of the FET can be calculated by the following formula:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\Theta JA}}$$

For the Fuji 2SK1388 FET, the RΘJA is 75°C/W. It is desirable for reliability that the junction temperature of the FET not exceed 120°C. If we assume that the ambient temperature is 25°C, then the power dissipation for the above assumption is:

$$P_D = \frac{120 - 25}{75} = 1.267W$$

By placing the FET down on the PC board and utilizing the power plane as a heatsink, we can reduce the RΘJA by a factor that corresponds to the surface area. For a 1 inch square area, the $R_{\Theta JA}$ would drop to around 40°C/W, in which case we would have:

$$P_D = \frac{120 - 25}{40(75)} = 2.37W$$

If we now calculate the power that the FET will dissipate at the rated 8A load, it will be given by:

$$P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$$

$$P = (64)(.037)\frac{3.3 + 0.4}{5 - 0.216} = 1.831W$$

Thus since the power at 8A is within the thermal guideline set above, we will not require a heat sink. For the case where the current is 11A, we can perform a similar calculation to arrive at the power dissipation:

$$P = (121)(.037)\frac{3.3 + 0.4}{5 - 0.407} = 3.607W$$

Clearly this power level will exceed our thermal guideline set above for 120°C maximum junction temperature and a single FET will require a heatsink or more surface area in order to reduce the $R_{\Theta JA}$.

Parallel FETs

An alternative method for reducing the power dissipation on the FET is to connect two power MOSFETs in parallel. In this case, the FETs will share the load current and can eliminate the need for a heatsink. One caution when designing with parallel FETs is to make sure that both the high current paths to the drain and from the source are equal, and that the gate drive signal to the FETs have the same propagation delay. These considerations are critical for the FETs to properly share the load current. An example of the thermal improvement with parallel MOSFETs is given below.

If we again assume that the load current will be 11Amps, the power dissipation for a single FET can be calculated as before:

$$P = (121)(.037)\frac{3.3 + 0.4}{5 - 0.407} = 3.607W$$

If we now utilize two FETs in parallel, effectively dropping the current through each FET. Thus the power dissipation of each FET is given by:

$$P = (5.5)(.037)\frac{3.3 + 0.4}{5 - 0.407} = 0.901W$$

This magnitude of improvement compounds upon itself because as the power dissipation of the FET drops, so does the Ron. This improvement will manifest itself in higher overall conversion efficiency for the regulator.

Schottky Diode

A similar analysis can be made for the fly-back schottky diode. In the non-synchronous design, the fly-back diode will have to carry the full current of the output load when the power MOSFET is turned off. Thus a thermal analysis is in order for this component as well. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_D = (I_{OUT})(V_F)T_{OFF}$$

If we use the example of a regulator supplying 11Amps to the load once more, we can calculate the power in a Motorola MBR2030CTL Power Rectifier. From the Motorola data book, the Vf of the diode at 11A is 0.5V. If we assume that the regulator is performing a 5V to 3.3V conversion, then the off time will be 1-Duty Cycle. (For 5V to 3.3V, the duty cycle is approximately 0.74):

$$P_D = (11)(0.5)(0.26) = 1.43W$$

Since this device is in a TO220 package, then we can compare this number to the number that was calculated above for the thermal resistance: maximum power for a free standing device = 1.267W. Since we calculated a higher number, we either have to add a heatsink, or mount the package down onto the PCB and use the PCB as a heatsink.

Characterizing and Debugging the Design

This section will provide a systematic approach to the debugging and characterization of the initial RC5035/36 regulator design. If all of the above design guide lines have been followed in the electrical and thermal design sections, then the debugging of the first design will be straight forward. We will discuss the equipment that is required for testing out the design, the methodology for debugging the design and last what is required to perform a thorough characterization of the design.

Equipment Required

The minimum set of equipment required is listed below:

1. 41/2 Digit DVM
2. Analog or Digital scope (100Mhz BW)
3. Current Load (Active)
4. PC “Silver Box” Power Supply

Additional equipment that can be useful in characterizing the performance of the regulator are:

1. Current Probe
2. Intel Transient Tester*

Debugging the First Design

We will treat the switching regulator design first, since there are more areas of concern with the switcher than with the linear. In debugging the switching regulator design, there is a methodology that needs to be followed in order to arrive at a successful conclusion. With the cost of the CPU being at least 2–3 times the cost of the PC motherboard, we need to ensure that the power supply for the CPU works properly and will not damage the CPU in any way. Thus a thorough evaluation of the power supply is required prior to plugging the CPU into the socket on the motherboard.

Initial Measurements

The initial measurements involve using the DVM to insure that the appropriate power is being applied to the proper pins of the RC5035/36/36.

1. **Check Power Supply** Using the DVM, check that there is +5V on the VCCA pin.(pin 6) Also check that there is +12V on the VCCL pin.(pin 11)
2. **Check Vref Test Point** Using the DVM, measure the voltage on the VERF pin.(pin 2) This voltage should be at 1.5V ±1%.
3. **Check Switch Control** Using the DVM, measure the voltage on the SWCTRL pin. (pin 16) A high level (+5V) on this pin will cause the switcher output of the RC5036 to be at +3.5V. (this is a no connect pin on the RC5035/36)
4. **Check VCCP** Using the DVM, measure the VCCP pin. (pin 10) This pin should be around 12V.
5. **Check VCCL** Using the DVM, measure the VCCL pin (pin 11). This pin should also be around 12V.
6. **Check LIN_EN** Using the DVM, measure the linear regulator enable pin 1. For the RC5036, a high level (+5V) on this pin will enable the linear regulator op-amp. (this pin is a no connect on the RC5035/36)
7. **Check VSC2** Using the DVM, measure the voltage on pin 13. This pin should measure very close to +5V for a no load condition on the linear regulator. A voltage difference between the VCC supply and VSC2 of more than 50mV will indicate a possible short circuit condition at the output of the linear regulator.
8. **Check the Linear Regulator Output** Using the DVM, measure the output voltage of the linear regulator. For the appropriate feedback resistors, the output voltage should be 3.3V ±3%.
9. **Check C_{EXT}** Using the oscilloscope, observe that there is a triangular wave shape on pin 15. The frequency of this pin will vary with the external capacitor selected and the output loading conditions.

*. At this writing there is no tester available for P55, however there are testers available from Intel for P54 and P6, thus we assume that a similar offering will be forthcoming.

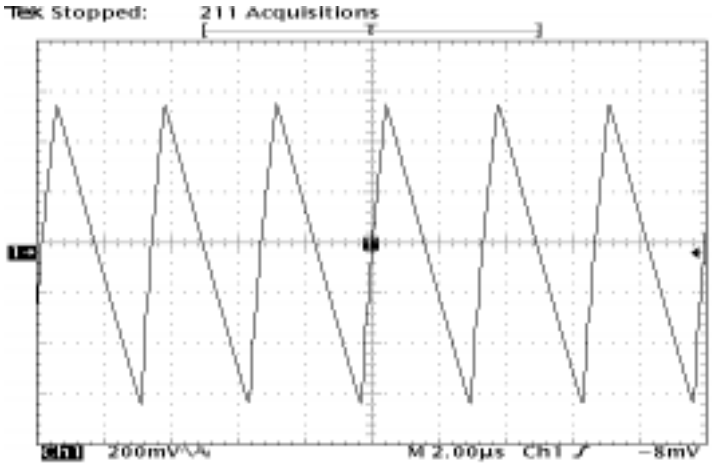

Figure 16 Timing Capacitor Waveform on Pin 15

10. **Check the Switcher Output Voltage** Using the DVM, measure the voltage at the output of the switching regulator circuit: after the sense resistor. For the RC5036, the output voltage should measure 3.5V ±3%. (the voltage output for the RC5035/36 and the RC5036 with SWCTRL low will be dependent on the external feedback resistor ratio) Using the active load connected to the output of the voltage regulator, apply a light loading condition, around 100mA, then again measure the switcher output. The voltage should remain at 3.5V.

If all of the above conditions look good, then we can proceed to the next step in the verification process; checking out the power supply design parameters. If there are problems with obtaining good results from the above steps, then most likely one or more of the external parts is either connected incorrectly or is faulty.

Step 2 Verification

1. **Load Regulation Check** This step involves using the active current load to check the load regulation of the supply through its specified load range. The active load should be connected to the output of the switching supply and the DVM used to measure the supply output voltage at the CPU socket. First set the active load to 0.5A, then measure Vout. Increment the active load to 1A, then 2A, etc. through the specified load range each time recording the output voltage. The load regulation is then calculated by the following equation:

$$LR = \frac{V_{OUT}(I_{MAX}) - V_{OUT}(I_{MIN})}{V_{OUT}(IDEAL)} \times 100 = \%$$

Both the switching supply and the linear regulator should be checked for load regulation through out the current range specified.

2. **Efficiency** The efficiency of the switching regulator can also be measured and compared to the calculated value to determine whether or not the components selected are operating within their specified ranges. Excessive efficiency losses would indicate that one or more components is being stressed beyond its specified temperature limits. The efficiency of a switching power supply is simply calculated from the relationship given below:

$$EFF = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \%$$

This efficiency number can be compared to the efficiency calculated from the estimations of the various losses in the components. The relationship is given below:

$$EFF = \frac{P_{OUT}}{P_{OUT} + PD_{TOTAL}} \times 100$$

Where PD_{TOTAL} is the sum of all of the power losses in the circuit.

- MOSFET loss: $PD_{FET} = I^2 \times R_{DS(ON)} \times DutyCycle$
- Diode loss: $P_{DIODE} = I \times V_F \times (1-DutyCycle)$
- Inductor loss: $PIND = I^2 \times R_{DC}$
- Sense Resistor loss: $P_{RSENSE} = I^2 \times R$
- Gate Drive loss: $PGATE = Q_G \times f \times V_{GS}$
- IC power loss: $P_{IC} = V_{CC} \times I_{CC}$

Transient Response Test This test evaluates the time that it takes for the regulator feedback loop to react to a step change in the output load current and then return to a specified steady-state voltage. This test is a measure of the regulator's ability to respond to a worst case change in current that might be demanded from the CPU, i.e. "sleep-full load". There are several available transient testers available from Intel for the P54. These test boards fit directly onto the CPU socket and involve a scope measurement similar to the one shown below. Contact Intel for information on Transient Testers. (See Figure 17).

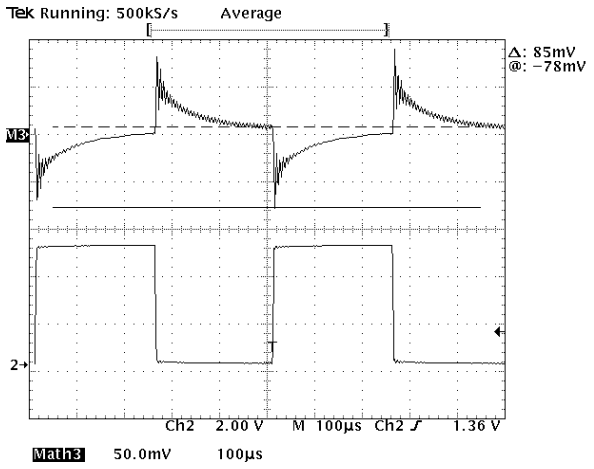

Figure 17 Transient Response of RC5036 Evaluation Board

Appendix A

Directory of Suppliers for Components
Dale Electronics, Inc.
E. Hwy. 50, PO Box 180
Yankton, SD 57078-0180
PH: (605) 665-9301

Fuji Electric
Collmer Semiconductor Inc.
14368 Proton Rd.
Dallas, Texas 75244
PH: (214)233-1589

Intel Corp.
5200 NE Elam Young Pkwy.
Hillsboro, OR. 97123
PH: (800) 843-4481 Tech. Support
for Power Validator

International Rectifier
233 Kansas St.
El Segundo, CA 90245
PH: (310) 322-3331

IRC Inc.
PO Box 1860
Boone, NC 28607
PH: (704) 264-8861

Mallory
North American Capacitor Co.
7545 Rockville Rd.
Indianapolis, IN 46214
PH: (317) 273-0090

Motorola Semiconductors
PO Box 20912
Phoenix, Arizona 85036
PH:(602) 897-5056

Nihon Inter Electronics Corp.
Quantum Marketing Int'l, Inc.
12900 Rolling Oaks Rd.
Caliente, CA 93518
PH: (805) 867-2555

Pulse Engineering
12220 World Trade Drive
San Diego, CA 92128
PH: (619) 674-8100

Sanyo Energy USA
2001 Sanyo Avenue
San Diego, CA 92173
PH: (619) 661-6620

Sumida Electric USA
5999 New Wilke Road Suite #110
Rolling Meadows, IL 60008
PH: (708) 956-0702

Xicon Capacitors
PO Box 170537
Arlington, Texas 76003
PH:(800) 628-0544

Appendix B

RC5036 Bill of Materials

BOM for RC5036 Application circuit #1 and #2				
Quantity	**Reference**	**Manufacturer**	**Part order #**	**Description**
4	C4,C5,C7,C14	Panasonic	ECU-V1H104ZFX	0.1uF 50V capacitor
1	C10	Panasonic	ECU-V1H153KBX	15nF capacitor
1	C6	Panasonic	ECU-V1H121JCG	120pF capacitor
1	C9	Panasonic	ECSH1CY105R	1uF 16V capacitor
4	C2,C3,C12,C13	Sanyo	6MV1500GX	1500uF 6.3V electrolytic capacitor 10mm x 20mm
1	C15	Sanyo	16MV330GX	330uF 16V electrolytic capacitor, 8mm x 15mm
1	DS1	Motorola	MBR1545CT	Schottky Diode, Motorola
1	L1	Pulse Engineering	PE-53682	4.7uH inductor
1	L2*	Pulse Engineering	PE-53680	1.32uH inductor
2	M1, M2	Fuji	2SK1388	N-Channel Logic Level Enhancement Mode MOSFET
1	Q1*	National	D44H11	NPN Power Transistor
1	R1	IRC	OAR-1	6 milliohm Iron Alloy resistor
1	R2	Panasonic	ERJ-6ENF1.74KV	1.74K 1% Resistor
1	R3	Panasonic	ERJ-6ENF2.00KV	2.00K 1% Resistor
1	R4	Panasonic	ERJ-6ENF12.1KV	12.1K, 1% Resistor
1	R5	Panasonic	ERJ-6ENF10.0KV	10K 1% resistor
1	R7	Panasonic	ERJ-6GEY100V	100 ohm 5% resistor
1	R6	IRC	OAR-1	7 milliohm Iron Alloy resistor
1	U1	Fairchild	RC5036M	Dual Regulator for P55 - Switching regulator + LDO Linear regulator

Appendix C

Selected Component Specifications

Table 1 Power MOSFETS

MOSFET Selection Table

Manufacturer and Model #	Conditions (Note 1)		$R_{DS, ON}$ (mΩ) Typ.	$R_{DS, ON}$ (mΩ) Max.	Package	Thermal Resistance	Price (note 2)	Availability (note 3)
Fuji	V_{GS}=4V, I_D=17.5A	T_J =25°C	25	37	TO-220	Φ_{JA}=75	$	Good
2SK1388		T_J =125°C	37	-				
Siliconix	V_{GS}=4.5V, I_D=5A	T_J =25°C	16.5	20	SO-8	Φ_{JA}=50	$$$	Good
SI4410DY		T_J =125°C	28	34	(SMD)			
National Semi NDP706AL	V_{GS}=5V, I_D=40A	T_J =25°C	13	15	TO-220	Φ_{JA}=62.5 Φ_{JC}=1.5	$$$	Long Lead Times
NDP706AEL		T_J =125°C	20	24				
National Semi NDP603AL	V_{GS}=4.5V, I_D=10A	T_J =25°C	31	40	TO-220	Φ_{JA}=62.5 Φ_{JC}=2.5	$	Long Lead Times
		T_J =125°C	42	54				
National Semi NDP606AL	V_{GS}=5V, I_D=24A	T_J =25°C	22	25	TO-220	Φ_{JA}=62.5 Φ_{JC}=1.5	$$	Long Lead Times
		T_J =125°C	33	40				
Motorola	V_{GS}=5V, I_D=37.5A	T_J =25°C	6	9	TO-263	Φ_{JA}=62.5	$$$	Unavailable
MTB75N03HDL		T_J =125°C	9.3	14	(D^2 PAK)	Φ_{JC}=1.0		
Int. Rectifier	V_{GS}=5V, I_D=31A	T_J =25°C	-	28	TO-220	Φ_{JA}=62.5	$	Good
IRLZ44		T_J =125°C	-	46		Φ_{JC}=1.0		

NOTES:

1. $R_{DS, ON}$ values at T_J = 125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.
2. Pricing information is used for relative purposes only. $ indicates the least expensive device, while $$$ indicates the most expensive.
3. Availability may differ from one source to another. Unavailable indicates a quoted lead time which is too long for a typical design schedule.

Table 2 Power Darlington Selection

Power Transistor Selection Table

Manufacturer and Model #	Conditions (Note 1)		$R_{DS, ON}$ (mΩ) Typ.	$R_{DS, ON}$ (mΩ) Max.	Package	Thermal Resistance	Price (note 2)	Availability (note 3)
			Typ.	Min.				
Various	Ic=4A, Vce=1V	T_J =25°C	80	40	TO-220	Φ_{JA}=75	$$	Good
D44HXX		T_J =125°C		-				
Motorola	Ic=3A, Vce=2V	T_J =25°C	80	40	TO-220	Φ_{JA}=62.5	$	Good
MJE15028								
		T_J =25°C			TO-220	Φ_{JA}=62.5	$	Good
		T_J =125°C				Φ_{JC}=1.0		

NOTES:

2. Pricing information is used for relative purposes only. $ indicates the least expensive device, while $$$ indicates the most expensive.
3. Availability may differ from one source to another. Unavailable indicates a quoted lead time which is too long for a typical design schedule.

Table 3 Power Magnetics, Inductors

Device	Mfgr.	Parameter	Conditions	Max Value	Units
CDHR127-1R3NC	Sumida	DCR	20ºC	.0101	W
PE-53680	Pulse Engr.	DCR	25ºC	.004	W

Table 4 Capacitors

Device	Mfgr.	Parameter	Conditions	Max Value	Units
20SA100M	Sanyo	ESR	100-300kHz	.037	W
6SA330M	Sanyo	ESR	100-300kHz	.035	W
1000μF	XICON	ESR	100-300kHz	0.15	W

Table 5 Schottky Diodes

Device	Mfgr.	Parameter	Conditions	Max Value	Units
C10T02QL	Nihon	Vf	If=5A	0.47	V
MBRB1545CT	Motorola	Vf	If=7.5A	0.57	V
MBRS140T3	Motorola	Vf	If=1A	0.6	V
EC10QS02L	Nihon	Vf	If=1A	0.45	V